IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 14920US01

In the Application of:

Anand Pande

U.S. Serial No.: 10/692,957

Filed: October 24, 2003

For: SYSTEM AND METHOD FOR DESIGNING DATA STRUCTURES

Examiner: Richard B. Franklin

Group Art Unit: 2181

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is a timely filed Appeal Brief. A Notice of Appeal was received by the United States Patent and Trademark Office on October 5, 2006 for the above-identified patent application. A Petition for a One-Month Extension is enclosed, thereby extending the deadline for filing an Appeal Brief to January 5, 2007.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals or interferences pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-19, 23 and 24 are being prosecuted in the present application. Claims 20-22 and 25-28 were withdrawn without prejudice. Claims 1-19, 23 and 24 stand rejected. The rejection of claims 1-19, 23 and 24 is being appealed.

STATUS OF AMENDMENTS

No amendments are pending in the present application.

SUMMARY OF CLAIMED SUBJECT MATTER

Some embodiments according to some aspects of the present invention may provide, for example, an asynchronous first-in-first-out (FIFO) data structure that includes, for example, a FIFO memory and a code generator as set forth in claim 1. The FIFO memory may have a depth d in which d is an integer. The code generator may be coupled, for example, to the FIFO memory and may provide, for example, a first code sequence of length 2d. The first code sequence may have, for example, a circular property and a Hamming length of one for any two consecutive codes of the first code sequence. The first code sequence may be generated from a second code sequence by removing one or more pairs of mirrored codes of the second code sequence.

Some embodiments according to some aspects of the present invention may provide, for example, a method for designing an asynchronous data structure as set forth in claim 16. The method may include, for example, one or more of the following: writing data to and reading data from a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers; reducing a first Gray-code sequence of length 2^n into a second Gray-code sequence of length 2d by removing one or more pairs of mirrored Gray-codes from the first Gray-code sequence; and using Gray codes of the second Gray-code sequence as Gray-code write pointers or Gray-code read pointers.

Some embodiments according to some aspects of the present invention may provide, for example, a method for designing an asynchronous data structure as set forth in claim 23. The method may include, for example, one or more of the following: writing data to and reading data from a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers; reducing a first code sequence of length 2^n into a second code sequence of length 2d by removing one or more pairs of mirrored codes from the first code sequence; and using codes of the second code sequence as code write pointers or code read pointers.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4, 12, 13, 16, 23 and 24 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 6,337,893 B1 to Timothy A. Pontius ("Pontius") in view of United States Patent No. 6,703,950 B2 to Cheng Yi ("Yi").

Whether claims 5-11, 14, 15 and 17-19 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Pontius in view of Yi, and further in view of United States Patent No. 6,810,468 B2 to Yuichiro Miyamoto et al. ("Miyamoto").

ARGUMENT

I. CLAIMS 1-4, 12 AND 13

Claims 1-4, 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being obvious over Pontius in view of Yi. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claim 1 recites "a FIFO memory having a depth d in which d is an integer; and a code generator coupled to the FIFO memory and providing a first code sequence of length 2d, the first code sequence having a circular property and a Hamming length of one for any two consecutive codes of the first code sequence, the first code sequence being generated from a second code sequence by removing one or more pairs of mirrored codes of the second code sequence".

In the Office Action Made Final mailed May 5, 2006 ("Office Action Made Final"), the Examiner alleges that "Pontius teaches a first-in-first-out (FIFO) memory having a length of d where d is an integer (Pontius; Col 4 Lines 37-46)". The Examiner also alleges that "Pontius also teaches generating a code sequence having a length of 2d (Pontius; Col 4 Lines 37-46)". Office Action Made Final at page 4.

However, the Examiner admits that Pontius has a plurality of teaching deficiencies.

For example, the Examiner admits that "Pontius does not teach that the code sequence is a first code sequence and is generated from a second code sequence by removing one or more pairs of mirrored codes from the second code sequence. The first code sequence has a circular property and a Hamming length of one for any two consecutive codes of the first code sequence". Office Action Made Final at page 4.

To make up for the teaching deficiencies of Pontius, the Examiner proposes to modify the teachings of Pontius in view of the teachings of Yi.

Appellant respectfully submits that the combination of Pontius in view of Yi is improper and that a rejection under 35 U.S.C. § 103(a) based, at least in part, on the combination of Pontius and Yi should be reversed by the Board.

M.P.E.P. § 2143.01(V) states that

> [i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

M.P.E.P. § 2143.01(V) at page 2100-129 (Rev. 5, Aug. 2006)(citing In re Gordon, 733 F. 2d 900, 221 U.S.P.Q.1125 (Fed. Cir. 1984)).

Appellant respectfully submits that Pontius states its *intended purpose* (in accordance with M.P.E.P. § 2143.01(V)) in, for example, the first paragraph of its Background of the Invention Section:

> [a] major objective of the invention is to provide for FIFO systems that permit simple detection of "full" and "empty" conditions when using read and write pointers with modulo numbers that are not powers of two.

Pontius at col. 1, lines 12-15.

An example of a "simple detection of 'full' and 'empty' conditions" is illustrated with respect to binary counters used with a FIFO depth that is a power of two. As discussed in the paragraph from col. 1, lines 40-53, "empty" is indicated when the pointers are equal and "full" is indicated when the difference between the points is the FIFO depth, which is half the point modulo number. "[If] binary counters are used, the FIFO is either full or empty when all the bits except the most significant bit are equal; the most significant bit distinguishes between full and empty". Pontius at col. 1, lines 47-50.

However, binary counters are defective in view of Pontius because more than one bit position must change simultaneously as the counter is counting which leads to the problem of transitional ambiguities. "A disadvantage of binary counters is that there can be considerable ambiguity when a count is read during a count transition". Pontius at col. 1, lines 58-60.

The solution that Pontius proposes to the problem of translational ambiguities is the use of a gray-code counter. "An alternative to binary code called 'gray code' requires a change in only one bit position in the event of a unit increment". Pontius at col. 2, lines 1-2.

The gray code counter used with a FIFO depth that is a power of two also provides for the "simple detection of 'full' and 'empty' conditions". "[G]ray code shares with binary code the characteristic that counts one-half the power-of-two counter modulus apart are readily determined. If two counts differ at and only at both of their two most significant bits, they are spaced apart by one-half the counter modulo number of counts apart. ... Thus, read and write counters based on power-of-two gray-code counters provide facile detection of full and empty FIFO conditions". Pontius at col. 2, lines 25-29 and 34-37.

However, Pontius identifies a critical problem with FIFO depths that are required to be a power of two: "[a] disadvantage of the Wingen gray-code counter as well as other gray-code counters ... is that, when the target FIFO depth is not a power of two, the FIFO design has excess capacity. For example, when a communication application only requires a FIFO depth of 78, the power-of-two limitation requires the use of an 128-address FIFO. ... The discrepancy between target and gray-code-imposed capacities can be much greater for larger FIFOs." Pontius at col. 2, lines 48-54 and 55-57.

Pontius further states that "[t]he excess capacity can be costly in terms of integrated-circuit area that might otherwise be devoted to other functions. The incorporating integrated circuit can be less functional or more costly as a result". Pontius at col. 2, lines 57-61.

Thus, Pontius extols the efficiencies and advantages of "non-power-of-two even modulo gray-code counters". Pontius at col. 2, lines 63-64.

However, the problem according to Pontius with using non-power-of-two even modulo gray-code counters is that "when the disclosed counters are one-half their modulo apart in their gray-code counts, the gray-code counts typically do not differ in any simple fashion". Pontius at col. 2, lines 65-67.

Pontius restates the intended purpose of the invention (in view of M.P.E.P. § 2143.01(V)):

> Thus, it is not straightforward to determine when a FIFO is full when two such counters are used for the read and write pointers. What is needed is a

> scaleable non-power-of-two gray-code counter design that provides for simple determination of when two counts half the counter modulo apart.

Pontius at col. 3, lines 3-8.

Having succinctly stated the intended purpose of the invention in Pontius, Appellant respectfully submits that proposed modification of Pontius in view of Yi would render the invention in Pontius unsatisfactory for its intended purpose. According to M.P.E.P. § 2143.01(V), such a proposed modification is prohibited and the combination of Pontius and Yi is improper.

Pontius at FIG. 1 illustrates the invention and the "simple detection of 'full' and 'empty' conditions when using read and write pointers with modulo numbers that are not powers of two". Pontius at col. 1, lines 12-15 (stating a major objective of the invention in Pontius).

As can be seen in FIG. 1, the "simple detection of 'full' and 'empty' conditions when using read and write pointers with modulo numbers that are not power of two" is to compare the most significant bit (MSB) in query 31, the next MSB in query 32 and the least significant bits (LSBs) in query 33. The output of the logical ANDs 36 and 37 detects and indicates the "full" and "empty" conditions.

The successful use of the "simple detection of 'full' and 'empty' conditions described in Pontius when using read and write pointers with modulo numbers that are not power of two" relies upon the method described in Pontius for generating sequential gray codes. The attention of the Board is respectfully drawn to the table in column 5 of Pontius as well as the discussions related thereto.

As can be ascertained by perusing the table in Pontius, a "full" condition can be detected if the pointers are at, for example, 1001 and 0101. In this case, referring to FIG.1, the MSBs are different, the second MSBs are different and the LSBs are the same, causing the logical AND 376 to indicate a "full" condition. If both pointers are at, for example, 1011, then the MSBs are the same, the second MSBs are the same and the LSBs are the same, causing the logical AND 37 to indicated an "empty" condition.

However, by using the teachings of Yi, an set of gray codes are generated that do not provide for a "simple detection of 'full' and 'empty' conditions when using read and write pointers with modulo numbers that are not powers of two".

Yi teaches that "whenever an equal number of codes are moved from immediately above and below the axis of reflection of a Gray code sequence, the resulting sequence will always be Gray code". Yi at col. 4, lines 16-19. This method of generating Gray code sequences is demonstrated in Table 3 of Yi.

Using the method that Yi teaches, a 4bit modulo 12 grey code counter sequence (note, for comparison, a 4bit modulo 12 grey code counter sequence is illustrated in the Table of Pontius) would look like this:

1000
1001
1011
1010
1110
1111
0111
0110
0010
0011
0001
0000

Appellant respectfully submits that Yi teaches a method for generating a 4 bit modulo 12 grey code counter sequence for which there is no "simple detection of 'full' and 'empty' conditions when using read and write pointers with modulo numbers that are not powers of two".

Appellant respectfully submits, for example, that there is no simple detection as described in Pontius of a "full" condition for the following sample pairs which should trigger a "full" condition: 1001 and 0110; 1011 and 0010; 1010 and 0011.

In other words, modifying the teachings of Pontius by the teachings of Yi leads to a modified invention in Pontius that is rendered unsatisfactory for its intended purpose (e.g., simple detection of "full" and "empty" conditions when using read and write pointers with modulo numbers that are not powers of two).

In view of the above arguments and rebuttal evidence, it is respectfully submitted that Pontius and Yi were improperly combined. The proposed modification of the invention in Pontius by the teachings of Yi renders the modified invention of Pontius unsatisfactory for its intended purpose.

In view of at least M.P.E.P. § 2143.01(V), Appellant respectfully submits that the obviousness rejection based, at least in part, on the combination of Pontius and Yi cannot be maintained.

It is respectfully requested that the Board reverse the rejection under 35 U.S.C. § 103(a) with respect to claim 1 and its rejected dependent claims (i.e., claims 2-4, 12 and 13).

II. CLAIM 16

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being obvious over Pontius in view of Yi. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claim 16 recites "writing data to and reading data from a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers; reducing a first Gray-code sequence of length 2^n into a second Gray-code sequence of length 2d by removing one or more pairs of mirrored Gray-codes from the first Gray-code sequence; and using Gray codes of the second Gray-code sequence as Gray-code write pointers or Gray-code read pointers".

In the Office Action Made Final, the Examiner alleges that "Pontius teaches a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers

(Pontius; Col 4 Lines 37-46). A code sequence of length 2d is generated and used as read and write pointers to the memory (Pontius; Figure 1 Items 10 and 20, Col 4 Lines 37-46)." Office Action Made Final at page 6.

However, the Examiner admits that Pontius has a plurality of teaching deficiencies.

For example, the Examiner admits that "Pontius does not teach reducing a first Gray-code sequence of length 2^n into a second Gary-code sequence of length 2d by removing one or more pairs of mirrored Gray-code sequences". Office Action Made Final at page 6.

To make up for the teaching deficiencies of Pontius, the Examiner proposes to modify the teachings of Pontius in view of the teachings of Yi.

Appellant respectfully submits that the combination of Pontius in view of Yi is improper and that a rejection under 35 U.S.C. § 103(a) based, at least in part, on the combination of Pontius and Yi should be reversed by the Board.

M.P.E.P. § 2143.01(V) states that

> [i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

M.P.E.P. § 2143.01(V) at page 2100-129 (Rev. 5, Aug. 2006)(citing In re Gordon, 733 F. 2d 900, 221 U.S.P.Q.1125 (Fed. Cir. 1984)).

Appellant respectfully submits that the proposed modification of the invention in Pontius by the teachings of Yi renders the modified invention in Pontius unsatisfactory for its intended purpose for at least the same or similar reasons as set forth with respect to claim 1.

Accordingly, Appellant makes the same or similar arguments with respect to claim 16 as are made above with respect to claim 1.

In view of the above arguments and rebuttal evidence, it is respectfully submitted that Pontius and Yi were improperly combined. The proposed modification of the invention in Pontius by the teachings of Yi renders the modified invention of Pontius unsatisfactory for its intended purpose.

In view of at least M.P.E.P. § 2143.01(V), Appellant respectfully submits that the obviousness rejection based, at least in part, on the combination of Pontius and Yi cannot be maintained.

It is respectfully requested that the Board reverse the rejection under 35 U.S.C. § 103(a) with respect to claim 16.

III. CLAIMS 23 AND 24

Claims 23 and 24 stand rejected under 35 U.S.C. § 103(a) as being obvious over Pontius in view of Yi. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claim 23 recites "writing data to and reading data from a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers; reducing a first code sequence of length 2^n into a second code sequence of length 2d by removing one or more pairs of mirrored codes from the first code sequence; and using codes of the second code sequence as code write pointers or code read pointers".

In the Office Action Made Final, the Examiner alleges that "Pontius teaches a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers (Pontius; Col 4 Lines 37-46). A code sequence of length 2d is generated and used as read and write pointers to the memory (Pontius; Figure 1 Items 10 and 20, Col 4 Lines 37-46)." Office Action Made Final at page 6.

However, the Examiner admits that Pontius has a plurality of teaching deficiencies.

For example, the Examiner admits that "Pontius does not teach reducing a first Gray-code sequence of length 2^n into a second Gary-code sequence of length 2d by removing one or more pairs of mirrored Gray-code sequences". Office Action Made Final at page 6.

To make up for the teaching deficiencies of Pontius, the Examiner proposes to modify the teachings of Pontius in view of the teachings of Yi.

Appellant respectfully submits that the combination of Pontius in view of Yi is improper and that a rejection under 35 U.S.C. § 103(a) based, at least in part, on the combination of Pontius and Yi should be reversed by the Board.

M.P.E.P. § 2143.01(V) states that

> [i]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.

M.P.E.P. § 2143.01(V) at page 2100-129 (Rev. 5, Aug. 2006)(citing In re Gordon, 733 F. 2d 900, 221 U.S.P.Q.1125 (Fed. Cir. 1984)).

Appellant respectfully submits that the proposed modification of the invention in Pontius by the teachings of Yi renders the modified invention in Pontius unsatisfactory for its intended purpose for at least the same or similar reasons as set forth with respect to claims 1 and 16.

Accordingly, Appellant makes the same or similar arguments with respect to claim 23 as are made above with respect to claims 1 and 23.

In view of the above arguments and rebuttal evidence, it is respectfully submitted that Pontius and Yi were improperly combined. The proposed modification of the invention in Pontius by the teachings of Yi renders the modified invention of Pontius unsatisfactory for its intended purpose.

In view of at least M.P.E.P. § 2143.01(V), Appellant respectfully submits that the obviousness rejection based, at least in part, on the combination of Pontius and Yi cannot be maintained.

It is respectfully requested that the Board reverse the rejection under 35 U.S.C. § 103(a) with respect to claim 23 and its rejected dependent claim (i.e., claim 24).

IV. <u>CLAIMS 5-11, 14 AND 15</u>

Claims 5-11, 14 and 15 stand rejected under 35 U.S.C. § 103(a) as being obvious over Pontius in view of Yi, and further in view of Miyamoto. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claims 5-11, 14 and 15 depend directly or indirectly from claim 1. Accordingly, the arguments made and the rebuttal evidence presented with respect to claim 1 are also made with respect to claims 5-11, 14 and 15.

For at least the above reasons, it is respectfully requested that the Board reverse the rejection under 35 U.S.C. § 103(a) with respect to claims 5-11, 14 and 15.

In addition, it is respectfully submitted that an obviousness rejection based on the combination of Pontius and Miyamoto or the combination of Yi and Miyamoto cannot be maintained.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination". M.P.E.P. § 2145(X)(D)(2) at page 2100-161 (Rev. 5, Aug. 2006)(citing In re Grasselli, 713 F. 2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)).

The teachings of Pontius and Yi teach away from the teachings of Miyamoto.

For example, Miyamoto teaches a FIFO circuit with a memory having addresses for 2^N words, N being an integer. See, e.g., Miyamoto at col. 2, lines 51 and 52; col. 3, lines 55 and 56.

On the other hand, Yi teaches away from using a full-length binary or Gray code sequences:

> The disadvantage of prior art Gray encoders/decoders is that they only operate on full-length binary code sequences. A full-length binary code sequence is defined as an N-digit binary code where the length (L) is equal to two to the power N:
>
> $$L = 2^N$$
>
> As an example of this full-length limitation, if the memory size needed for FIFO memory control logic is 18, the bit number N for the address bus has to be at least 5 ($2^4 \leq 18 \leq 2^5$). However, with N = 5, the $L = 2^N$ limitation for prior art Gray encoders/decoders requires that the memory size be 32, nearly twice the memory required by the memory control logic.
>
> In view of the foregoing, it can be appreciated that a need exists for a Gray encoder/decoder that can encode/decode Gray code sequences that have lengths less than 2N.

Yi at col. 2, lines 26-42.

Likewise, Pontius also teaches away from the teachings of Miyamoto. Pontius disparages the 2^N depth FIFO of Miyamoto because such FIFO designs have excess capacity.

> A disadvantage of the Wingen gray-code counter as well as other gray-code counters ... is that, when the target FIFO depth is not a power of two, the FIFO design has excess capacity. For example, when a communication application only requires a FIFO depth of 78, the power-of-two limitation requires the use of an 128-address FIFO. ... The discrepancy between target and gray-code-imposed capacities can be much greater for larger FIFOs.

Pontius at col. 2, lines 48-54 and 55-57.

Pontius further states that "[t]he excess capacity can be costly in terms of integrated-circuit area that might otherwise be devoted to other functions. The incorporating integrated circuit can be less functional or more costly as a result". Pontius at col. 2, lines 57-61.

Thus, it is respectfully submitted that Miyamoto cannot be properly combined with Pontius and Yi where Pontius teaches away from Miyamoto and Yi teaches away from Miyamoto.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection based on either Pontius and Miyamoto or Yi and Miyamoto.

For at least the foregoing, it is respectfully requested that the rejection under 35 U.S.C. § 103(a) be reversed with respect to claims 5-11, 14 and 15.

V. <u>CLAIMS 17-19</u>

Claims 17-19 stand rejected under 35 U.S.C. § 103(a) as being obvious over Pontius in view of Yi, and further in view of Miyamoto. It is respectfully requested that the Board reverse the rejection for at least the reasons as set forth below.

Claims 17-19 depend from claim 16. Accordingly, the arguments made and the rebuttal evidence presented with respect to claim 16 are also made with respect to claims 17-19.

For at least the above reasons, it is respectfully requested that the Board reverse the rejection under 35 U.S.C. § 103(a) with respect to claims 17-19.

In addition, it is respectfully submitted that an obviousness rejection based on the combination of Pontius and Miyamoto or the combination of Yi and Miyamoto cannot be maintained.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination". M.P.E.P. § 2145(X)(D)(2) at page 2100-161 (Rev. 5, Aug. 2006)(citing In re Grasselli, 713 F. 2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)).

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For example, Miyamoto teaches a FIFO circuit with a memory having addresses for 2^N words, N being an integer. See, e.g., Miyamoto at col. 2, lines 51 and 52; col. 3, lines 55 and 56.

On the other hand, Yi teaches away from using a full-length binary or Gray code sequences:

> The disadvantage of prior art Gray encoders/decoders is that they only operate on full-length binary code sequences. A full-length binary code sequence is defined as an N-digit binary code where the length (L) is equal to two to the power N:
>
> $$L = 2^N$$
>
> As an example of this full-length limitation, if the memory size needed for FIFO memory control logic is 18, the bit number N for the address bus has to be at least 5 ($2^4 \leq 18 \leq 2^5$). However, with N = 5, the $L = 2^N$ limitation for prior art Gray encoders/decoders requires that the memory size be 32, nearly twice the memory required by the memory control logic.
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> In view of the foregoing, it can be appreciated that a need exists for a Gray encoder/decoder that can encode/decode Gray code sequences that have lengths less than 2N.

Yi at col. 2, lines 26-42.

Likewise, Pontius also teaches away from the teachings of Miyamoto. Pontius disparages the 2^N depth FIFO of Miyamoto because such FIFO designs have excess capacity.

> A disadvantage of the Wingen gray-code counter as well as other gray-code counters ... is that, when the target FIFO depth is not a power of two, the FIFO design has excess capacity. For example, when a communication application only requires a FIFO depth of 78, the power-of-two limitation requires the use of an 128-address FIFO. ... The discrepancy between target and gray-code-imposed capacities can be much greater for larger FIFOs.

Pontius at col. 2, lines 48-54 and 55-57.

Pontius further states that "[t]he excess capacity can be costly in terms of integrated-circuit area that might otherwise be devoted to other functions. The incorporating integrated circuit can be less functional or more costly as a result". Pontius at col. 2, lines 57-61.

Thus, it is respectfully submitted that Miyamoto cannot be properly combined with Pontius and Yi where Pontius teaches away from Miyamoto and Yi teaches away from Miyamoto.

For at least the above reasons, it is respectfully requested that the Board reverse the obviousness rejection based on either Pontius and Miyamoto or Yi and Miyamoto.

For at least the foregoing, it is respectfully requested that the rejection under 35 U.S.C. § 103(a) be reversed with respect to claims 17-19.

V. CONCLUSION

For the foregoing reasons, it is believed that claims 1-19, 23 and 24 are patentable over the alleged prior art of record. Reversal of the Examiner's rejection of claims 1-19, 23 and 24 is therefore respectfully requested, thereby placing claims 1-19, 23 and 24 in condition for allowance. Accordingly, issuance of a patent on the application is therefore respectfully requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: January 5, 2007

Respectfully submitted,

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CLAIMS APPENDIX

The following claims are involved in this appeal:

1. An asynchronous first-in-first-out (FIFO) data structure, comprising:

a FIFO memory having a depth d in which d is an integer; and

a code generator coupled to the FIFO memory and providing a first code sequence of length 2d, the first code sequence having a circular property and a Hamming length of one for any two consecutive codes of the first code sequence, the first code sequence being generated from a second code sequence by removing one or more pairs of mirrored codes of the second code sequence.

2. The data structure according to claim 1, wherein the second code sequence has the circular property and the Hamming length of one for any two consecutive codes of the second code sequence.

3. The data structure according to claim 1, wherein the first code sequence is a Gray-code sequence.

4. The data structure according to claim 1, wherein the second code sequence is a Gray-code sequence.

5. The data structure according to claim 1, wherein the code generator is coupled to a write pointer which, in turn, is coupled to the FIFO memory.

6. The data structure according to claim 5, wherein the write pointer is coupled to the FIFO memory via at least one of a converter and a look-up table.

7. The data structure according to claim 6, wherein the converter comprises a Gray-to-binary converter.

8. The data structure according to claim 1, wherein the code generator is coupled to a read pointer which, in turn, is coupled to the FIFO memory.

9. The data structure according to claim 8, wherein the read pointer is coupled to the FIFO memory via a Gray-to-binary converter.

10. The data structure according to claim 1, wherein the code generator is coupled to a read pointer which, in turn, is coupled to the FIFO memory.

11. The data structure according to claim 10, wherein the FIFO memory comprises a bank of registers.

12. The data structure according to claim 1, wherein the FIFO memory comprises a write data input port and a read data output port.

13. The data structure according to claim 1, wherein the FIFO memory comprises a write pointer input and a read pointer input.

14. The data structure according to claim 1, wherein the asynchronous FIFO data structure comprises a write clock domain and a read clock domain.

15. The data structure according to claim 14,
wherein the write clock domain comprises a write clock,
wherein the read clock domain comprises a read clock, and
wherein the read clock and the write clock are asynchronous.

16. A method for designing an asynchronous data structure, comprising:
writing data to and reading data from a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers;

reducing a first Gray-code sequence of length 2^n into a second Gray-code sequence of length 2d by removing one or more pairs of mirrored Gray-codes from the first Gray-code sequence; and

using Gray codes of the second Gray-code sequence as Gray-code write pointers or Gray-code read pointers.

17. The method according to claim 16, wherein the writing and the reading are asynchronous operations.

18. The method according to claim 16, wherein the writing and the reading are part of a first-in-first-out (FIFO) process.

19. The method according to claim 16, wherein the asynchronous data structure comprises a FIFO data structure.

23. A method for designing an asynchronous data structure, comprising:

writing data to and reading data from a memory of depth d in which d is not equal to a value 2^n and in which d and n are integers;

reducing a first code sequence of length 2^n into a second code sequence of length 2d by removing one or more pairs of mirrored codes from the first code sequence; and

using codes of the second code sequence as code write pointers or code read pointers.

24. The method according to claim 23, wherein at least one of the first code sequence and the second code sequence has at least one of a closed property and a Hamming distance of one.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.